What is claimed is:

[Claim 1] 1. An optical proximity correction (OPC) method for reducing optical proximity effect occurring in a pattern transferring process, the method comprising:

providing a photo-mask;

providing an original photo-mask pattern predetermined to be formed on a surface of the photo-mask, the original photo-mask pattern comprising at least one integrated circuit layout composed of dense figures and at least one isolated figure;

providing a plurality of dummy patterns to surround the isolated figure to reduce the difference in pattern density of the original photo-mask pattern, a transmitted light of the dummy patterns providing a phase difference of 0 or 180 degrees relative to a transmitted light of the integrated circuit layout, and the integrated circuit layout and the plurality of dummy patterns together composing a corrected photo-mask pattern; and

forming the corrected photo-mask pattern on the surface of the photo-mask.

[Claim 2] 2. The method of claim 1, wherein the integrated circuit layout is transferred to a photoresist layer formed on a surface of a substrate by the pattern transferring process.

[Claim 3] 3. The method of claim 2, wherein the plurality of dummy patterns are nonprintable dummy patterns and not transferred to the photoresist layer during the pattern transferring process.

[Claim 4] 4. The method of claim 3, wherein the shapes, the dimensions and the numbers of the dummy patterns are designed according to exposure wave length and numerical apertures of the pattern transferring process and the materials included in the photoresist layer.

[Claim 5] 5. The method of claim 4, wherein the edge length of each dummy pattern is a multiple of exposure wave length, and the multiple is less than 0.6.

[Claim 6] 6. The method of claim 4, wherein the distance between each dummy pattern is a multiple of exposure wave length, and the multiple ranges between 0.3 and 2.0.

[Claim 7] 7. The method of claim 4, wherein the least distance between the dummy patterns and the integrated circuit layout is a multiple of exposure wave length, the multiple ranges between 0.4 and 2.0.

[Claim 8] 8. An optical proximity correction method for reducing optical proximity effect occurring in a pattern transferring process, the method comprising:

providing a photo-mask;

providing an integrated circuit layout predetermined to be formed on a surface of the photo-mask, the integrated circuit layout comprising dense figures and at least one isolated figure;

performing a partial OPC of the integrated circuit layout for obtaining a corrected integrated circuit layout; and

forming the corrected integrated circuit layout on the surface of the photo-mask and forming a plurality of dummy patterns surrounding the isolated figure, the dummy patterns being capable of reducing the difference in pattern density of the corrected integrated circuit layout, and a transmitted light of the dummy patterns providing a phase difference of 0 or 180 degrees relative to a transmitted light of the corrected integrated circuit layout.

[Claim 9] 9. The method of claim 8, wherein the partial OPC is used to modify pattern transferring defects of the integrated circuit layout comprising right-angled corner rounding, line end shortening, and line width increasing/decreasing.

[Claim 10] 10. The method of claim 8, wherein the plurality of dummy patterns are nonprintable dummy patterns and not transferred to a photoresist layer formed on a surface of a substrate during the pattern transferring process, however, the integrated circuit layout is transferred to the photoresist layer by the pattern transferring process.

[Claim 11] 11. The method of claim 10, wherein the shapes, the dimensions and the numbers of the dummy patterns are designed according to exposure wave length and numerical apertures of the pattern transferring process and the materials included in the photoresist layer.

[Claim 12] 12. The method of claim 11, wherein the edge length of each dummy pattern is a multiple of exposure wave length, and the multiple is less than 0.6.

[Claim 13] 13. The method of claim 11, wherein the distance between each dummy pattern is a multiple of exposure wave length, and the multiple ranges between 0.3 and 2.0.

[Claim 14] 14. The method of claim 11, wherein the least distance between the dummy patterns and the integrated circuit layout is a multiple of exposure wave length, the multiple ranges between 0.4 and 2.0.